WHAT IS CLAIMED IS:

1. An apparatus for timing recovery for a receiver in a communication system, said apparatus comprising:

a phase estimator having an input for receiving phase information corresponding to a remote clock signal associated with a data signal and operable to determine a phase error with respect to said remote clock signal and a local clock signal, said phase estimator further operable to translate said phase error for timing correction of a local clock signal and issue a corresponding correction signal; and

a first clock modifier having an input for receiving said local clock signal and operable to apply a first phase modifier responsive to said issued correction signal, said first clock modifier further having an output for issuing a synchronized clock signal.

2. The apparatus of Claim 1, wherein said synchronized clock signal is received as a drive signal by an analog-to-digital converter which converts said data signal at a sampling frequency responsive to said synchronized clock signal.

3. The apparatus of Claim 1, wherein said first clock modifier further includes a delay line having a plurality of delay elements, wherein each delay element introduces a predetermined clock jitter to said local clock signal.

4. The apparatus of Claim 3, wherein clock jitters are applied to said local clock signal in an equal distribution over a time duration.

5. The apparatus of Claim 3, wherein said delay elements are serially coupled

6. The apparatus of Claim 5, wherein said first clock modifier further includes a phase selector having an input for receiving a tapped coupling from each of said delay elements, a serial coupling of all delay elements, and said local clock signal, wherein said phase selector is further operable to select a clock jitter responsive to said issued correction signal.

7. The apparatus of Claim 1, further including a second clock modifier having an input for receiving said local clock signal and operable to apply a second phase modifier to said local clock signal responsive to said issued correction signal in combination with said first clock modifier applying said first phase modifier.

8. The apparatus of Claim 7, wherein said first clock modifier includes a delay line having a plurality of serially coupled delay elements, wherein each delay element introduces a predetermined phase delay to said local clock signal, wherein said second clock modifier introduces a greater phase clock jitter to said local clock signal than a clock jitter introduced by said first clock modifier.

9. The apparatus of Claim 8, wherein clock jitters are applied to said local clock signal in an equal distribution over a time duration.

10. The apparatus of Claim 8, wherein said first clock modifier further includes a phase selector having an input for receiving said serially coupled delay elements, a tapped coupling from each of said delay elements, and a clock signal from said second clock modifier, wherein said phase selector is further operable to select a clock jitter responsive to said issued correction signal.

11. A system for synchronizing a local clock signal with a remote clock signal from phase information associated with a data signal transmitted in a communication network, said system comprising:

a signal converter having an input for receiving said data signal and operable to convert said data signal at a sampling frequency responsive to a synchronized clock signal;

a phase estimator having an input for receiving said phase information corresponding to said remote clock signal and operable to determine a phase error with respect to said remote clock signal, said phase estimator further operable to translate said phase error for timing correction of a local clock signal and issue a corresponding correction signal; and

a first clock modifier having an input for receiving said local clock signal and operable to apply a first phase modifier responsive to said issued correction signal, said first clock modifier further having an output coupled to said signal converter for issuing a synchronized clock signal.

12. The system of Claim 11, wherein said first clock modifier further includes a delay line having a plurality of delay elements, wherein each delay element introduces a predetermined clock jitter to said local clock signal.

13. The system of Claim 12, wherein clock jitters are applied to said local clock signal in an equal distribution over a time duration.

14. The system of Claim 12, wherein said delay elements are serially coupled.

15. The system of Claim 11, wherein said first clock modifier further includes a phase selector having an input for receiving a tapped coupling from each of said delay elements, a serial coupling of all delay elements, and said local clock signal, wherein said phase selector is further operable to select a clock jitter responsive to said issued correction signal.

16. The system of Claim 11, further including a second clock modifier having an input for receiving said local clock signal and operable to apply a second phase modifier to said local clock signal responsive to said issued correction signal in combination with said first clock modifier applying said first phase modifier.

17. The system of Claim 16, wherein said first clock modifier includes a delay line having a plurality of serially coupled delay elements, wherein each delay element introduces a predetermined clock jitter to said local clock signal, wherein said second clock modifier introduces a greater clock jitter to said local clock signal than a clock jitter introduced by said first clock modifier.

18. The system of Claim 17, wherein clock jitters are applied to said local clock signal in an equal distribution over a time duration.

19. A method of synchronizing a local clock signal with a remote clock signal from phase information associated with a data signal transmitted in a communication network, comprising:

determining a phase error with respect to said remote clock signal;

determining a number of clock jitters to be applied over a data frame of a time duration to synchronize a local clock signal with said remote clock signal; and

applying said clock jitters to said local clock signal in an equal distribution spacing over said time duration and centered within a boundary of said data frame, wherein a time between clock jitters is equal to said time duration divide by said determined number of clock jitters.

20. The method of Claim 19, wherein a clock jitter is applied to said local clock signal from a tapped delay line comprising a plurality of serially coupled delay elements coupled to a phase selector, wherein said delay elements are further individually coupled to said phase selector, said phase selector operable to apply said distributed clock jitters responsive to said determined phase error.